IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Atty. Docket

WILLIAM REDMAN-WHITE ET AL GB 000101

Serial No.

Filed: CONCURRENTLY

DATA DECODING

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

3. (Amended) An arrangement as claimed in Claim 1 including indication means for indicating which of the plurality of inputs is the largest.

5. (Amended) An arrangement as claimed in Claim 1 including a current sensing and reproduction arrangement coupled between the output of the summing arrangement and the output of the arrangement.

9. (Amended) An arrangement as claimed in Claim 7 comprising a second capacitor connected across the first transistor via a third switch and a fourth switch connected between the second capacitor and the gate electrode of the second transistor wherein the third switch is closed during the subsequent sample period and the fourth switch is closed during the one sample period.

10. (Amended) An arrangement as claimed in Claim 1 comprising a comparator for determining when the largest of the input currents is greater than a predetermined value and producing an output indicative thereof and means for subtracting the predetermined value from the output current.

12. (Amended) An arrangement as claimed in Claim 7 in comprising a third transistor having its gate electrode connected to the gate electrode of the second transistor and its drain electrode connected to a second output of the arrangement.

14. (Amended) A Viterbi decoder comprising a trellis network interconnecting a plurality of arrangements as claimed in Claim 1, the plurality of inputs to each of the arrangements being derived from outputs of one or more of the arrangements as defined by the connection trellis, a corresponding plurality of probability signal generators for generating a probability signal indicating the probability that a received signal corresponds to a valid signal value, the outputs of the probability signal generators being fed to the respective further inputs of the arrangements, wherein at least one of the arrangements includes indicating means for indicating which of the plurality of inputs is the largest and the indicating means is connected to a serial in serial out shift register whose output provides the decoded data.

16. (Amended) Any novel feature or any novel combination of features disclosed herein either explicitly or implicitly whether or not it relates to the same invention as that claimed in Claim 1.

<u>REMARKS</u>

The claims have been amended in order to reformat the claims to delete all multiple dependencies prior to calculation of the filing fee and place the instant application in standard U.S. format.

Entry of this amendment prior to calculating the filing fee is respectfully requested.

Respectfully submitted,

By____________________

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APPENDIX

3. (Amended) An arrangement as claimed in Claim 1 ~~or Claim 2~~ including indication means for indicating which of the plurality of inputs is the largest.

5. (Amended) An arrangement as claimed in Claim 1 ~~any preceding claim~~ including a current sensing and reproduction arrangement coupled between the output of the summing arrangement and the output of the arrangement.

9. (Amended) An arrangement as claimed in Claim 7 ~~or Claim 8~~ comprising a second capacitor connected across the first transistor via a third switch and a fourth switch connected between the second capacitor and the gate electrode of the second transistor wherein the third switch is closed during the subsequent sample period and the fourth switch is closed during the one sample period.

10. (Amended) An arrangement as claimed in Claim 1 ~~any of Claims 5 to 7 or in Claim 9 when dependent on Claim 7~~ comprising a comparator for determining when the largest of the input currents is greater than a predetermined value and producing an output indicative thereof and means for subtracting the predetermined value from the output current.

12. (Amended) An arrangement as claimed in Claim 7 ~~any of Claims 7 to 11~~ in comprising a third transistor having its gate electrode connected to the gate electrode of the second transistor and its drain electrode connected to a second output of the arrangement.

14. (Amended) A Viterbi decoder comprising a trellis network interconnecting a plurality of arrangements as claimed in Claim 1 ~~any preceding claim~~, the plurality of inputs to each of the arrangements being derived from outputs of one or more of the arrangements as defined by the connection trellis, a corresponding plurality of probability signal generators for generating a probability signal indicating the probability that a received signal corresponds to a valid signal value, the outputs of the probability signal generators being fed to the respective further inputs of the arrangements, wherein at least one of the arrangements includes indicating means for indicating which of the plurality of inputs is the largest and the indicating means is connected to a serial in serial out shift register whose output provides the decoded data.

16. (Amended) Any novel feature or any novel combination of features disclosed herein either explicitly or implicitly whether or not it relates to the same invention as that claimed in Claim 1 ~~any preceding claim~~.